TAIWAN SEMICONDUCTOR

AN-1011

PerFET™ Advantage Introduction

Content

1. Introduction

Taiwan Semiconductor introduces PerFET™, a family of products built on proprietary device structures and processes that enable exceptionally low on-state resistance and switching figure-of-merit (FOM – $R_{DS(on)}$*Q). The achievement of 50% $R_{DS(on)}$ and 40% FOM reduction compared to our previous technology puts this portfolio at the industry leading edge of performance. This initial 40V N-channel platform includes options for both standard (10V) and logic level (5V) gate-drive requirements while preserving rugged safe-operating resistance to switching voltage transients and avalanche concerns in switching applications.

With the ultralow Ron and low gate charge features, PerFET™ Power MOSFETs show outstanding performance in applications such as switch mode power supplies (SMPS), DC to DC converter, motor controller, inverters and Automotive…

1.1 Differences between Trench and PerFET™ generations

Here compare the closest RDS(on) value between the Trench and PerFET™ which is 3.2m ohm, parameters shown in table 1, and will describe how differences in the following sections.

Table 1: Overview of the datasheet

Technology	**Trench**	**PerFET™**	
	TSM033NB04LCR	TSM032NH04LCR	
Parameter	**TYP**		UNIT
Gate Threshold Voltage, $V_{GS(TH)}$	1 (Min) / 1.8 /2.5 (Max)	1.4 (Min) / 1.8 /2.2 (Max)	V
Drain-Source On-State Resistance, $R_{DS(on)}$	3.3 (at 10Vgs, I_D = 21A)	3.2 (at 10Vgs, I_D = 50A)	mΩ
	4 (at 4.5Vgs, I_D = 19A)	4.2 (at 4.5Vgs, I_D = 50A)	
Forward Transconductance, gfs	63	93	S
Total Gate Charge, Qg @10Vgs	79	50	nC
Total Gate Charge, Qg @4.5Vgs	40	23.7	

Gate-Source Charge, Qgs	12	9.8	nC
Gate-Drain Charge, Qgd	19	6.9	
Input Capacitance, Ciss	4456	3007	pF
Output Capacitance, Coss	475	562	
Reverse Transfer Capacitance, Crss	276	34	
Gate Resistance, Rg	1.5	0.7	Ω

2. Key parameters improvement

2.1 $R_{DS(on)}$ dependence on temperature

To measure Drain-Source on-resistance, $R_{DS(on)}$, with a given current source, I_D, measure the voltage drop across Drain-Source, V_{DS}. And after that, through the equation, $R_{DS(on)} = V_{DS} / I_D$, $R_{DS(on)}$ is observed. I_D effect on the $R_{DS(on)}$ value is minimal, and the temperature coefficient (K) is more important. The TSC MOSFET datasheet shows the RDS(on) vs TJ curve characteristics, indicating that the $R_{DS(on)}$ is a positive temperature coefficient.

$K = \frac{R_{DS(on)\ at\ T_J}}{R_{ds(on)\ at\ 25℃}}$ ... the temperature coefficient

Figure 1 shows that the PerFET™'s temperature coefficient difference is minimal, so our two products with the $R_{DS(on)}$ will be different at higher temperatures. E.g. for TSM032NH04LCR is 1.5 times which is better than 1.72 times (TSM033NB04LCR) at T_J = 125℃. There,

$3.2mΩ \times 1.5 = 4.8mΩ$ ... TSM032NH04LCR, T_J = 125℃

$3.3mΩ \times 1.72 = 5.7mΩ$ ... TSM033NB04LCR, T_J = 125℃

When selecting MOSFETs for a power supply system, it is important to consider the surrounding temperature.

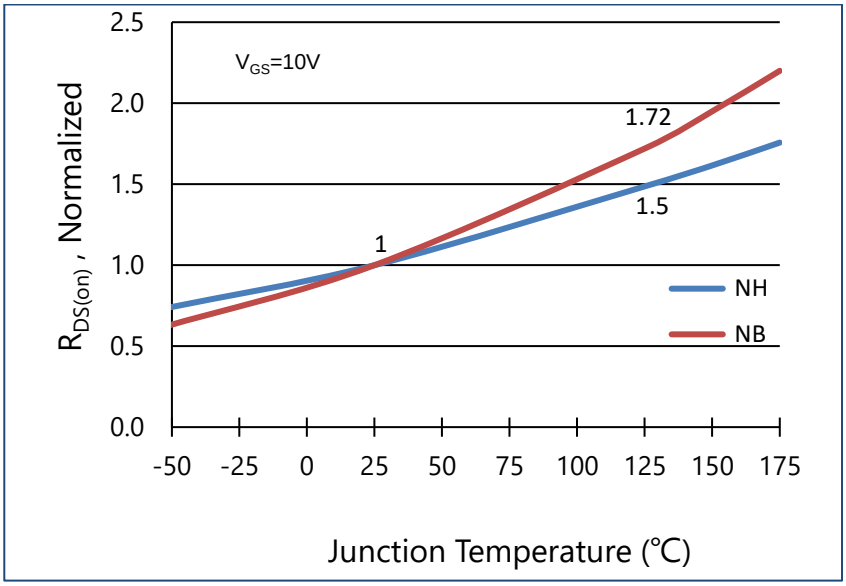

Figure 1 $R_{DS(on)}$ normalized vs. Junction Temperature

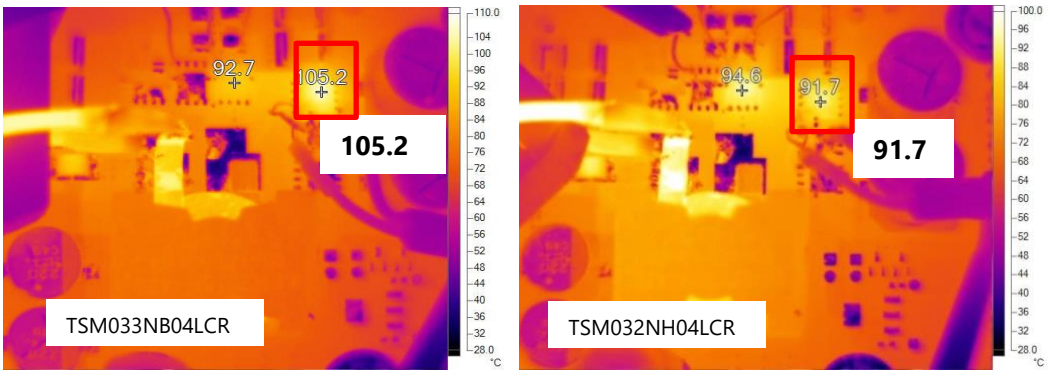

Figure 2 Thermal images compared with PerFET™ at DC-DC converter

Figure 2 is the TSM033NB04LCR compared with the TSM032NH04LCR apply in the SYNC-BUCK converter with 340kHz switching frequency, this thermal image exhibits the lower temperature with PerFET™ application.

2.2 Gate Threshold voltage of limitation

To improve the immunity to against the noise or unwanted induced voltage on the gate. PerFET™ 40VPower MOSFETs series increase the logic level (LL) MOSFETs $V_{GS(TH).Min}$ to 1.4V and this helps to avoid the MOSFET be turned on falsely. It brings higher efficiency and reliability to many automotive and industrial applications.

Logic level (LL):

TSM032NH04LCR

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	1.4	1.8	2.2	V

TSM033NB04LCR

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	1	1.6	2.5	V

Figure 3 $V_{GS(TH)}$ limitation

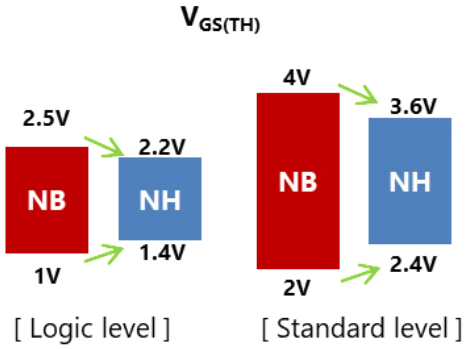

Figure 4 Narrow down $V_{GS(TH)}$ deviation of PerFET™

2.3 Capacitance of Ciss, Crss and Coss

Ciss, Coss, and Crss directly influence the switching performance. To optimize for high switching applications, PerFET™ power MOSFETs have lower Ciss, Crss, and Coss. Figure 5 is the typical characteristic curve.

Ciss = Cgs +Cgd ;

Crss = Cgd

Coss = Cds +Cgd

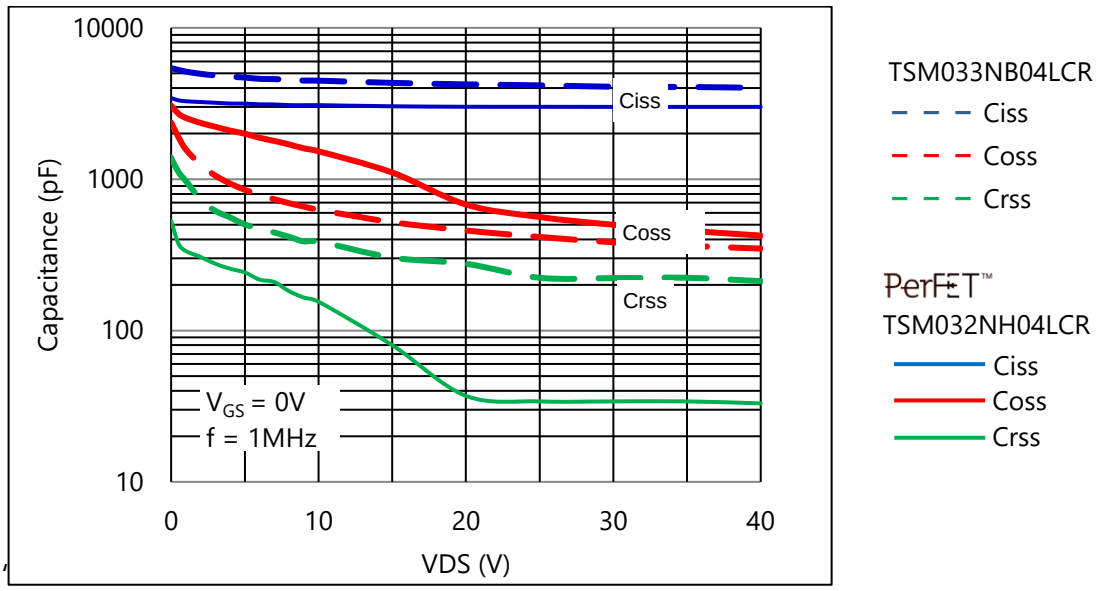

Figure 5 Capacitance characteristic curve

2.4 Gate Charge: Qg, Qgs and Qgd

Gate charge includes three specified values, Qg, Qgs and Qgd. Qgs denotes Gate to Source charge. Qgd denotes gate to drain charge, which is also called the miller effect charge. Qg denotes the total gate charge for full turn-on the MOSFET. Figure 6 illustrates the definitions of gate charge characteristics.

PerFET™ has a lower gate charge (Qg, Qgs, Qgd) than TSC's Trench, the time (t_0 ~ t_4) required for the switching operations depends on the gate charge and the gate driver sink and source current capability; figure 6 illustrates the device switching dissipation from turn off to turn-on characteristics and vice versa.

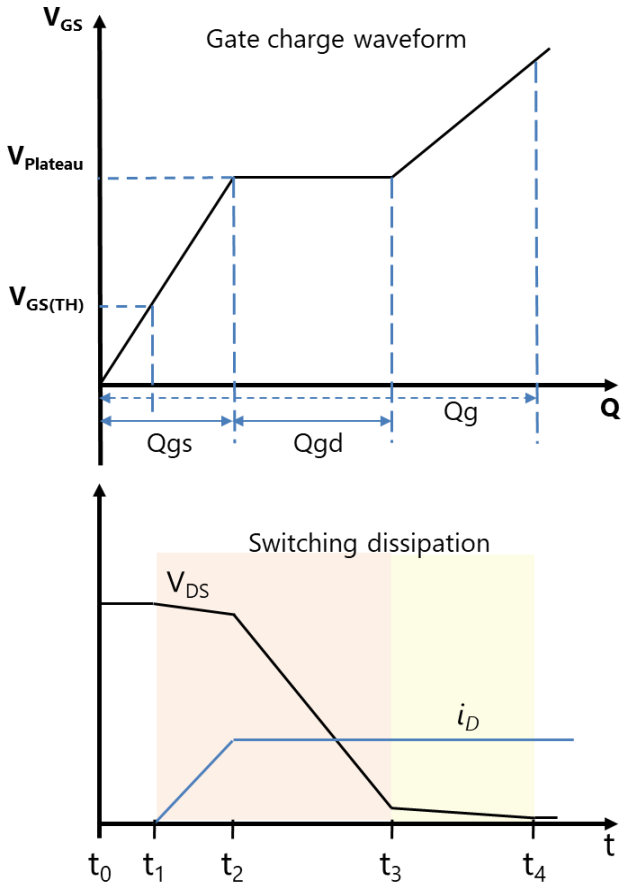

Figure 6 MOSFET switching-on waveform

Figure 7 measures two products' gate charge waveform in the test circuit, and PerFET™ reduces 31% at gate charge, improving the switching time. So, it reduces the switching dissipation and increases efficiency, especially in the higher switching frequency system. Another tip of gate charge for picking up a MOSFET in Half-bridge power system design is that the ratio of Qgd/Qgs is lower than 1 to prevent the circuit from shoot through, and PerFET™ is optimized, e.g. Qgd/Qgs =6.9/9.8 =0.7< 1.

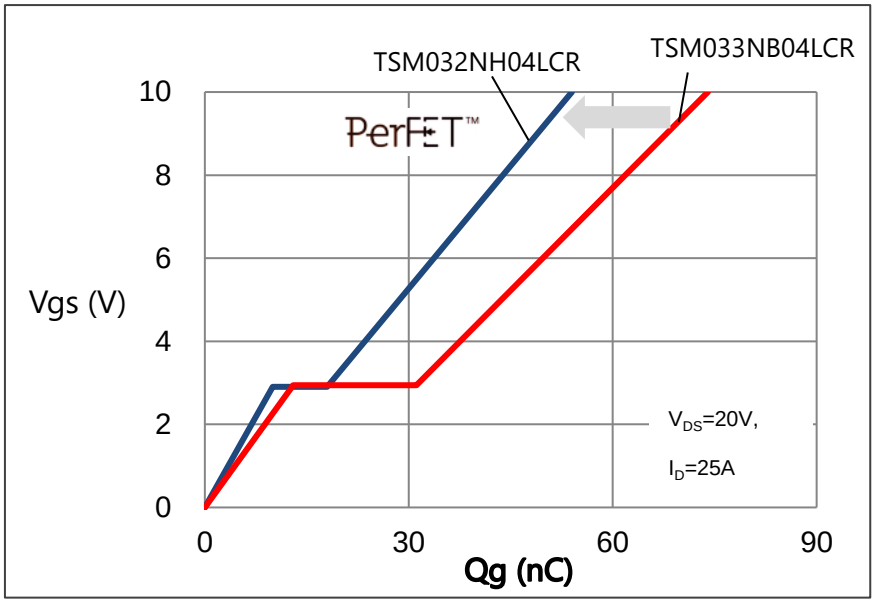

Figure 7 PerFET^{TM} gate charge curve

Figure 8 is a measuring Vgs waveform on the same power converter, TSM032NH04LCR's rise time is 68ns better than 103ns (TSM033NB04LCR).

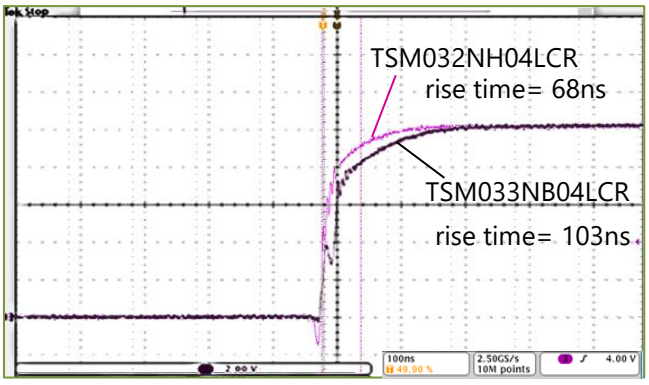

Figure 8 V_{GS} measuring waveform on DC-DC converter

3. Key benefits

3.1 Offers immunity to uncontrol turn-on

After parameters introducing, PerFET™ has a lower Qgd/Qgs ratio, and higher $V_{GS(TH)\_Min}$, this is optimized for immunity against uncontrol turn-on, which often occurs in real-world applications and increases power consumption, leading to overheating or even damage.

The behavior of induced turn-on involves a high Vds/dt causing a voltage spike at the gate due to the capacitive voltage divider formed by the Cgd and Cgs. This could be enough to turn the MOSFET on, as shown in Figure 9. So, a higher $V_{GS(TH)\_Min}$ prevents gate voltage spikes that uncontrol turn-on. In addition, a lower Qgd/Qgs ratio (Cgd/Cgs divider ratio) reduces the induced voltage spikes, further contributing to the robustness against uncontrol turn-on.

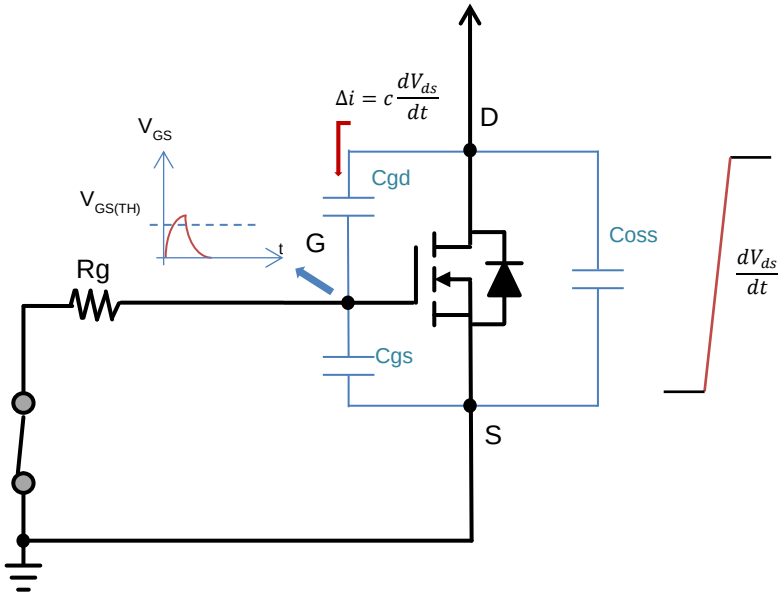

Figure 9 dVds/dt to induce voltage spike on the Vgs

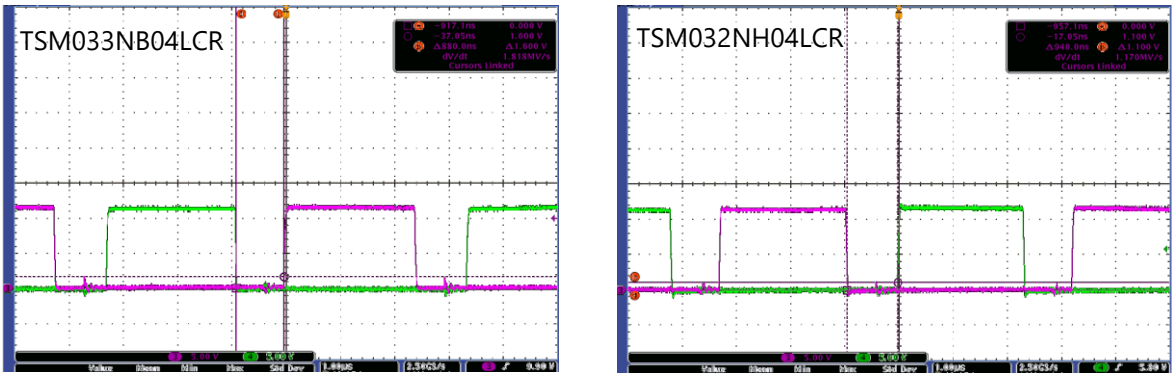

Figure 10 V_{GS} measuring waveform on the power supply

Figure 10 is a measuring Vgs waveform on the same power converter, TSM032NH04LCR's induced voltage is 1.1V lower than 1.6V (TSM033NB04LCR). TSM032NH04LCR's induced voltage is low than the minimum $V_{GS(TH)}$= 1.4V. As mentioned in section 2.2, which helps to avoid the MOSFET be turned on falsely. Therefore, PerFET™ (TSM032NH04LCR) is suitable for higher power, high switching frequency applications.

4. Wettable flank package

Automatic Optical Inspection (AOI) is used for many applications during the assembly process to ensure quality. Packages with wettable flank leads are designed to improve solder joint reliability and AOI's accuracy. The PDFN56U wettable flank package is designed Leadframe to gain more plating area after the singulation process, it provides good adhesion between the Tin solder and the Leadframe pin after the reflow process. The solder tin amount combined more with the Leadframe pin, the AOI judgment pass yield rate becomes more and can guarantee package device solder reliability well. PerFET™ goes to standard grade on PDN56U wettable flank package, figure 11 illustrates the difference.

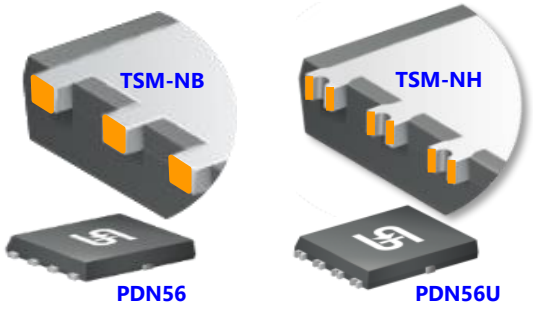

Figure 11 PDFN56 compared with PDFN56U (wettable flank package)

4.1 Examination

4.1.1 The optical microscope examined the pin solder joint status (Figure 12). The wettable frank PDFN56U tin soap profile is more significant than the standard PDFN56.

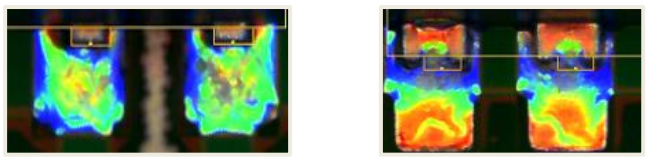

Figure 12 Standard PDFN56 solder status compared with PDFN56U

4.1.2 TSC applies cross-section to examine the solder combination profile as below. Compared to the solder wetting, a higher height "H" means a better solder effect. PDFN56U wetting height "H" is higher than standard PDFN56. These wettable frank packages wetting height even cover the whole lead height, more detailed experiments can reference in TSC's application note AN-1009.

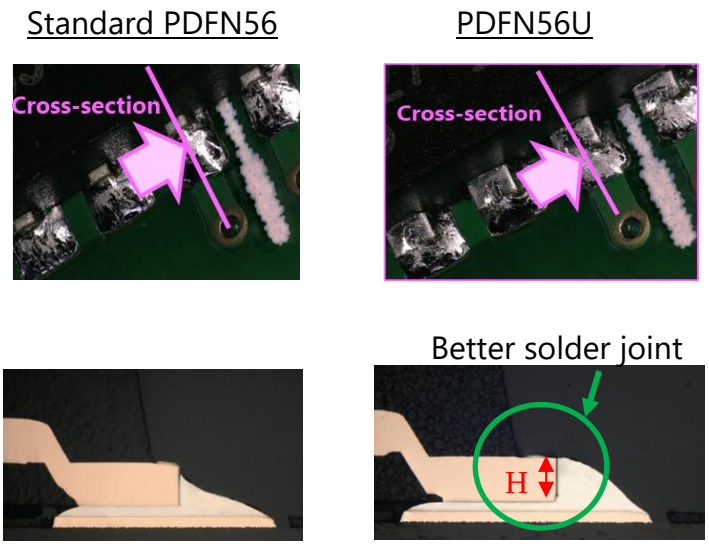

Figure 13 Standard PDFN56 cross-section compared with PDFN56U

5. Summary

PerFET^{TM} has better $R_{DS(on)}$ temperature coefficient (K) to carry good thermal performance in the high temperature, better $V_{GS(TH)}$ deviation that is suitable between the MOSFET in parallel at high-power system; Lower capacitance and gate charge to reduce the switching dissipation and improve efficiency at higher switching frequency application. And Lower Qgd/Qgs ratio (Cgd/Cgs divider ratio) reduces the gate voltage spikes, further devoting to robustness against uncontrol turn-on. In the wettable flank package on PDN56U benefits many applications during the assembly process to ensure quality.

Reference

1. AN-1001: Understanding Power MOSFET Parameters
2. AN-1009: Wettable flank packages of DFN56U, SMPC4.6U enable AOI choice
3. TSM033NB04LCR : datasheet
4. TSM032NH04LCR : datasheet

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Notice

Application Notes serve only as hints for the implementation of the product and should not be considered in any way as a description or warranty of certain conditions, functions, or quality of the product. The recipient of this application note must follow the datasheet specification before implementing the product.

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